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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte GILBERT WOLRICH, MATTHEW J. ADILETTA,
WILLIAM R. WHEELER, DEBRA BERNSTEIN, and
DONALD F. HOOPER

Appeal 2009-004498
Application 10/069,352
Technology Center 2100

Decided: March 29, 2010

Before JAMES D. THOMAS, LEE E. BARRETT, and STEPHEN C. SIU, *Administrative Patent Judges*.

THOMAS, *Administrative Patent Judge.*

DECISION ON APPEAL

STATEMENT OF THE CASE

This is an appeal under 35 U.S.C. § 134(a) from the Examiner's final rejection of claims 1-6, 8-11, 14, 17, 20-25, 27-30, 33, and 36. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

INVENTION

> A method of operating a processor to perform direct write operations to the processor's registers, including, for example the processor's control and status registers. The method includes receiving data in a processing thread having a processing thread number and loading the data into selected bits of a register according to the processing thread number.

(Abst.)

REPRESENTATIVE CLAIM

> 1. A method of operating a multi-threaded processor comprising:
>
> receiving data specified by execution of a fast-write instruction in one of multiple threads processing on the multi-threaded processor, the one of the multiple threads identified by a processing thread number, the fast-write instruction further specifying a register, the register having multiple groups of bits, each group of bits associated with a corresponding thread of the multiple threads processing on the multi-threaded processor;
>
> selecting a group of bits associated with the one of the multiple threads, the group of bits being selected from the multiple groups of bits of the register specified by the fast-write instruction according to the processing thread number; and loading the data into the bit positions of the selected group of bits of the register.

PRIOR ART AND EXAMINER'S REJECTIONS

The Examiner relies on the following reference as evidence of anticipation and unpatentability:

Bhattacharya	5,704,054	Dec. 30, 1997

The Examiner relies upon this reference as extrinsic evidence:

Sproull et al., "The Counterflow Pipeline Processor Architecture," IEEE DESIGN & TEST OF COMPUTERS FALL 1994, pp.48-59.

Claims 1, 2, 6, 8, 9, 20, 21, 25, 27 and 28 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Bhattacharya. The remaining claims on appeal, claims 3-5, 10, 11, 14, 17, 22-24, 29, 30, 33, and 36 stand rejected under 35 U.S.C. § 103. As evidence of obviousness, the Examiner relies upon Bhattacharya alone.

CLAIM GROUPINGS

Based upon Appellants' arguments in the principal Brief on appeal, Appellants argue independent claim 1 as representative of the subject matter of independent claims 1 and 20. Appellants present arguments as to dependent claim 2 as representative of the subject matter of claims 2 and 21. The same may be said of claim 6 as representative of the subject matter of claims 6 and 25. No arguments are presented as to any remaining claim within the rejection under 35 U.S.C. § 102. Correspondingly, Appellants rely for patentability within the claims listed for the rejection under 35 U.S.C. § 103 based upon those arguments presented with respect to their parent independent claims within the first stated rejection under 35 U.S.C. § 102.

ISSUE

Has the Examiner erred in finding that Bhattacharya teaches the selecting clause of representative independent claim 1 on appeal?

FINDINGS OF FACT

Bhattacharya's column 2, lines 6-10 make reference to a Sproull publication in which a prior art ASIC (application specific integrated circuit) platform has a high degree of pipelining in its architecture.

With respect to this prior art Sproull publication and the prior art showing in Bhattacharya's Figure 1, it is stated at column 2, lines 30-42:

> When an instruction is received in instruction recover module 20 from instruction cache 18, it is passed to a decode module 30. In turn, decode module 30 transmits to register file 12 an indication of the data that is required to enable execution of the decoded instruction. This identification data is termed "binding" by Sproull et al. and results in the launch, by register file 12, of the requested data left into the processor's central pipeline (i.e. from right to left). Each instruction carries with it a "binding" for its source operands and its destination in the pipeline. Each binding associates a data value with a register name and thus enables register file 12 to identify the proper data to be launched. Bindings are matched base upon matches of register names.

Correspondingly, this description is enhanced by the following at column 3, lines, 3-13:

> Instruction register 40 further includes an operand code section 56 for defining an operation to be performed with respect to data held in source registers 46 and 48. Each of the source and destination registers includes a section 58 that carries a binding value (e.g. a register name in register file 12).

> In similar manner, result registers 60 and 62 also contain binding value sections 64. By comparison of binding values 58 and 64 in logic circuit 44, a pipeline stage is able to determine which data passing through result register 42 is to be associated with an instruction in instruction register 40.

With this background in mind, Bhattacharya's Figures 5-7 are pertinent to the issues in this appeal. Figure 5 depicts a schematic of a CFPP (counterflow pipeline processor) architecture of which Figures 6 shows a detail of a pipeline stage 100/102 in Figure 5. A plurality of threads is illustrated in Figure 5 in various stages of processing within respective portions of pipeline stages illustrated. The generically illustrated sequencer module SEG in Figure 5 is further detailed in Figure 6. The Examiner therefore relies upon the following teachings at column 6, lines 25-57 with respect to Figures 5 and 6:

> Turning to FIG. 5, a portion of a pipeline embodying the invention has been modified to enable multi-threaded execution of independent data processing actions. In FIG. 5, details of individual pipeline stages and siding logical blocks have been eliminated. Between each pair of successive pipeline stages (e.g. 100 and 102), there resides a sequencer module 104 which controls movement of instructions and results between pipeline stages. In FIG. 6 an exemplary pipeline stage is shown that is employed in the multi-thread pipeline structure of FIG. 5. Each source and destination latch in instruction register 40 is provided with plural address positions 106. Result latches 42 are similarly provided with plural address positions 108. Assuming that there are three threads being executed on a time-shared basis, each instruction register 40 and result register 42 must contain at least three separate address positions to hold source and destination/result values form the respective threads.
>
> Sequencer modules 110 and 112 respectively provide address designations in succeeding pipeline stages for both the result values flowing in the result pipeline and the instructions

> flowing in the instruction pipeline. For instance, sequencer 110 will provide output addresses in a next pipeline stage to which result values residing in result register 42 will be directed. Similarly, sequencer 112 provides an input address for results coming from a prior pipeline stage. Sequencer 110 provides an input address for instructions entering instruction register 40 and sequencer 122 provides output addresses to which the instruction in register 40 will be directed in a subsequent pipeline stage.
>
> Assuming, as indicated above, that there are three threads in process, sequencers 110 and 112 sequence in a round-robin manner through the three threads and cause movement of individual instructions/results of each thread.

Figure 7 is a block diagram of corresponding siding logic employed within Bhattacharya's invention. Illustrated in this figure is an input interface and thread selection logic 120 that operates upon respective register files 122, 124, 126, with intermediate combinational logic, as well as latches forming respective register addresses to the respective register files. This is discussed at column 7, lines 15-34, which we reproduce here:

> In FIG. 7, "siding" logic stages are illustrated which are adapted for use in a multi-threaded pipeline environment. In such case, an instruction is fed from the pipeline to an input interface and thread selection logic module 120. That module assigns a set of register addresses into which the instruction values are to be inserted in register files 122, 124, 126, etc. as the particular instruction is being executed by intervening combinational siding blocks. As each new thread instruction is received from the pipeline, a new series of addresses are generated and inserted into latches 128, 130, 132 so as to enable proper placement of result values in the respective register files. In such manner, addresses are pipelined in the siding logical blocks so as to enable proper placement of individual thread results. After the results are generated, they are passed back to the pipeline via output interface 134. Logical operations are

> thus performed on individual instructions from separate threads, while maintaining a differentiation therebetween and assuring a proper sequencing of the results through the register files included in the siding.

PRINCIPLES OF LAW

Anticipation

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co.*, 814 F.2d 628, 631 (Fed. Cir. 1987) (citation omitted). Analysis of whether a claim is patentable over the prior art under 35 U.S.C. § 102 begins with a determination of the scope of the claim. We determine the scope of the claims in patent applications not solely on the basis of the claim language, but upon giving claims their broadest reasonable construction in light of the specification as it would be interpreted by one of ordinary skill in the art. *In re Am. Acad. of Sci. Tech Ctr.*, 367 F.3d 1359, 1364 (Fed. Cir. 2004). The properly interpreted claim must then be compared with the prior art.

ANALYSIS

We refer to, rely on, and adopt the Examiner's findings and conclusions set forth in the Answer. The Reply Brief does not question or contest the Examiner's reliance upon the Sproull publication as extrinsic evidence in the responsive arguments portion of the Answer beginning at page 8. This Sproull publication is specifically referenced at column 2 of Bhattacharya as we noted in our findings of fact.

As our reproduced portions at columns 2 and 3 of Bhattacharya set forth the background and prior art approaches in Bhattacharya, this reference appears to modify the approach taken by Sproull "such that each register has N sections, one section for each thread" as expressed at the bottom of page 9 of the Answer, which approach is consistent with the statement of the rejection at pages 3 and 4 of it. A subtle distinction is brought up by the Examiner at this location in the Answer such that prior art Figure 2 merely shows an instruction containing one value per register 52 associated with prior art Figure 2 of Bhattacharya, "whereas FIG. 6 shows N values per register, one per each thread."

We generally agree with the Examiner's reliance upon the column 6 discussion that we have reproduced in our Findings of Facts. These views appear to be confirmed by our reference to Figure 7 in our Findings of Fact and the noted discussion that we reproduced there as well. Appellants' Brief and Reply Brief do not actually challenge the Examiner's characterization that Bhattacharya teaches overall that each register has N sections, one section for each thread. Therefore, we agree with the Examiner's view that the selection clause is reasonably shown by the Examiner to have been anticipated by Bhattacharya.

We do not agree with Appellants' characterization at the bottom of page 1 of the Reply Brief that the so-called fast-write instruction has not been met by this reference. Contrary to what has been asserted here, no argument has been made in the principal Brief that the fast-write instruction per se, alone, recited in claim 1 is not taught. The arguments in the principal Brief at pages 8, 9 and 10 merely focus upon the entire selecting clause. Moreover, the claim itself does not recite any unique properties about the

fast-write instruction itself such that it is merely a label for an instruction that is well represented by the instructions already taught in Bhattacharya.

On the one hand, we agree with Appellants' criticisms at page 2 of the Reply Brief regarding the Examiner's characterization at page 12 of the Answer of assigning thread numbers mentally. On the other hand, Appellants have incompletely reproduced at page 2 of the Reply Brief the Examiner's remarks from page 12 of the Answer. The Examiner goes on to indicate beginning with the sentence bridging pages 12 and 13 of the Answer that "despite this mental identification, the system of Bhattacharya must be able to distinguish (identify) each thread to determine group of bits to select and write to the result register. The mental identification explanation merely points out the broadness of the claim language."

Overall, Appellants' arguments in the principal Brief directed to representative independent claim 1 as well as their responsive arguments in the Reply Brief do not convince us of any error in the Examiner's position with respect to this claim. We reach a similar result with respective claim 2 which merely recites a label identified as a "control and status register (CSR)." There is ample evidence that the Examiner has identified and we have identified in our Finding of Facts portion in this Opinion that justifies a consideration that the registers we and the Examiner have identified perform a function of controlling and indicating status of the instruction pipelining and multi-threading operations in Bhattacharya.

Lastly, we turn to the features recited in dependent claim 6 which indicates that the at least one of the multiple threads is processed on a micro engine of a multi-threaded processor. We agree with the Examiner reliance upon Figure 5 to indicate a pipeline processing functionality corresponding

to a micro-engine as noted at page 15 of the Answer. We briefly described in our Findings of Fact the composition of Figure 5 and it certainly includes more than the mere sequencer modules discussed by Appellants at page 12 of the principal Brief on appeal. Since Figure 5 depicts the sequencers as well as the pipeline stages themselves, the combination of teachings and showings in that entire figure may be fairly characterized as micro-engines to the extent claimed as the Examiner has indicated in the Answer.

CONCLUSION AND DECISION

Appellants have not shown that the Examiner erred in finding that Bhattacharya teaches the selecting clause of representative independent claim 1 on appeal. Likewise, Appellants have not shown that the Examiner erred in concluding that the subject matter of representative dependent claims 2 and 6 are also anticipated by this reference. We therefore affirm the rejection of these claims and all other claims on appeal respectively rejected under 35 U.S.C. §§ 102 and 103.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv) (2009).

AFFIRMED

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